CLAIMS

What is claimed is:

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1.   A communication system, comprising:

a.   a memory structure receiving and storing undecoded symbols, each of the undecoded symbols having a unique pointer associated therewith and one of the undecoded symbols being a most

10   likely symbol; and

b.   a pointer selector processing the unique pointers according to a predetermined selection operation and selecting a most likely pointer uniquely associated with the most likely symbol, the decoder outputting the most likely symbol thereby.

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2.   The communication system of claim 1, wherein the predetermined selection operation is a shuffle exchange operation and the pointer selector is a shuffle exchange network.

20   3.   The communication system of claim 1, wherein the undecoded symbols are representative of potential received signals.

4.   The communication system of claim 2, wherein the system conforms to IEEE Standard 802.3ab.

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5.   The communication system of claim 2, wherein the memory structure and the pointer selector comprise a trellis decoder.

6.   The communication system of claim 5, wherein the trellis

30   decoder comprises a Viterbi decoder.

7.   The communication system of claim 6, wherein the undecoded symbols are four-dimensional (4-D) symbols.

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8.   The communication system of claim 7, wherein the predefined symbol states comprise eight symbol states.

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9.   The communication system of claim 1, further comprising a multiplexor coupled with the memory structure and the pointer selector, the multiplexor selecting the most likely symbol responsive to activation by the most likely pointer.

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10.   A communication system, comprising:

a.   a memory structure receiving and storing undecoded symbols, each of the undecoded symbols being representative of potential received symbols conforming to IEEE Standard 802.3ab,

15   each of the undecoded symbols having a unique pointer associated therewith and one of the undecoded symbols being a most likely symbol; and

b.   a shuffle exchange network processing the unique pointers according to a shuffle exchange operation and selecting a most

20   likely pointer uniquely associated with the most likely symbol, the decoder outputting the most likely symbol thereby;

wherein the memory structure and shuffle exchange network comprise a trellis decoder.

25   11.   A decoder, comprising:

a.   a memory structure receiving and storing undecoded symbols, each of the undecoded symbols having a unique pointer associated therewith and one of the undecoded symbols being a most likely symbol; and

30   b.   a pointer selector processing the unique pointers according to a predetermined selection operation and selecting a most likely pointer uniquely associated with the most likely symbol, the decoder outputting the most likely symbol thereby.

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12. The decoder of claim 11, wherein the predetermined selection operation is a shuffle exchange operation and the pointer selector is a shuffle exchange network.

13. The decoder of claim 11, wherein the undecoded symbols are representative of potential received signals.

14. The decoder of claim 12, wherein the potential received symbols are constituent of predefined symbol states.

15. The decoder of claim 12, wherein the decoder comprises a trellis decoder.

16. The decoder of claim 15, wherein the decoder comprises a Viterbi decoder.

17. The decoder of claim 14, wherein the undecoded symbols are four-dimensional (4-D) symbols.

18. The decoder of claim 17, wherein the predefined symbol states comprise eight symbol states.

19. The decoder of claim 11, further comprising a multiplexor coupled with the memory structure and the pointer selector, the multiplexor selecting the most likely symbol responsive to activation by the most likely pointer.

20. A decoder, comprising a survivor memory unit (SMU), the SMU storing information to be decoded, the information including undecoded symbols and pointers representative of particular ones of the undecoded symbols, the SMU performing a predetermined index sorting operation on ones of the pointers to a select one of the undecoded symbols.

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21.   The decoder of claim 20, further comprising a shuffle-exchange network (SEN), and wherein the predetermined pointer sorting operation is a shuffle-exchange operation.

22.   The decoder of claim 20, wherein each of the undecoded symbols is a 4-dimensional symbol, and each of the pointers is a three-bit pointer representative of a unique symbol state.

23.   The decoder of claim 21, further comprising a memory structure storing the undecoded symbols therein during the shuffle-exchange operation.

24.   The decoder of claim 23, further comprising an Add-Compare-Select Unit (ACS) operably coupled with, and transmitting undecoded symbols to, the SMU; and the ACS choosing a selected one of the pointers unique to a desired decoded symbol.

25.   The decoder of claim 23, wherein the memory structure is a FIFO.

26.   The decoder of claim 23, wherein the memory structure is a dual-port RAM.

27.   The decoder of claim 23, wherein the memory structure is a single-port RAM, the single-port RAM being capable of a read/modify/write operation in a single symbol period.

28.   The decoder of claim 23, wherein the memory structure is a dynamic RAM.

29.   The decoder of claim 25, wherein the FIFO is a dual-port RAM.

30. A decoder, comprising:

a. a memory structure receiving potential symbols, each of the symbols having a unique pointer associated therewith;

b. a shuffle exchange network (SEN), the SEN performing shuffle exchange operations on the unique pointers and producing a most likely pointer corresponding to a most likely symbol; and

c. a first memory multiplexor coupled to the memory structure and the SEN, the first memory multiplexor being responsive to the most likely pointer, thereby producing the most likely symbol at the memory structure output.

31. The decoder of claim 30, wherein each of the memory structure and the SEN have an input, and further comprising a preprocessing shuffle exchange unit coupled to the input of the memory structure and the SEN, the preprocessing shuffle exchange unit receiving original potential symbols and unique pointers and selecting a set of most likely potential symbols and a set of most likely unique pointers therefrom.

32. The decoder of claim 31, further comprising a trellis decoder.

33. The decoder of claim 32, further comprising a Viterbi decoder.

34. The decoder of claim 30, further comprising an add-select-compare (ACS) unit which generates potential symbols for input to the memory structure, generates unique pointers associated with the potential symbols for input to the SEN, and generates a most likely pointer selection signal to which the first multiplexor is responsive.

35.   The decoder of claim 34, further comprising a branch metric unit (BMU) computing the transition costs for sequential symbol transitions in a trellis encoding scheme, generating the potential symbols states representative of the potential symbols thereby, the potential symbol states being input to the ACS for selection of the potential symbols.

36.   A method for processing symbolic communication signals, comprising:

    a.   receiving potential symbols including a most likely symbol;

    b.   associating each of the received potential symbols with a unique pointer;

    c.   processing the unique pointers associated with selected ones of the received potential symbols to determine a most likely pointer using a predetermined selection operation; and

    d.   selecting the most likely symbol using the most likely pointer.

37.   The method of claim 36, further comprising storing the potential symbols in a memory structure.

38.   The method of claim 37, wherein the memory structure is capable of performing a read operation and a write operation in one clock cycle.

39.   The method of claim 36, wherein the predetermined selection operation is a shuffle exchange operation.

40.   The method of claim 36, wherein the received potential symbols are 4-D undecoded symbols.

41. The method of claim 40, wherein the method is constituent
5   of a communication scheme according to IEEE Standard 802.3ab.

42. A communication system, comprising:
a.   a branch metric unit for computing branch-metrics for all
transitions of a trellis of a used code;
10   b.   an add-select-compare unit, coupled to the branch metric
unit, for adding branch metrics to path metrics for all possible
states, the path metrics corresponding to a likelihood of a
received symbol sequence to end in a state associated with the path
metrics; and
15   c.   a survivor memory unit, coupled to the add-select-compare
unit, for merging a four-dimensional (4-D) output symbol with a
shuffle-exchange algorithm, the shuffle-exchange algorithm
operative on an index representation of a 4-D symbol.

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